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CS 5780

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Lab 6 Pre-Lab

1. What is hysteresis and how does it help prevent bad behavior on digital inputs?

It is a basic improvement over the simple thresholding method. It changes the voltage threshold depending on the currently detected digital state; this therefore makes it impossible for a signal to consistently hang around the specified trigger point. It can help prevent bad behavior on digital inputs by once an input signal is interpreted as digital high, the threshold for transitioning to digital low goes down, and then requires an extremely low value to move to the low state. Thus preventing an input signal with voltages close to the threshold to cause rapid transitions since tiny ripples can move the value above and below the trigger point.

1. What is quantization?

It is the process of mapping a high-resolution signal to a manageable lower-resolution signal.

1. What does Nyquist theory explain? What is the problem with sampling a signal too slowly?

It explains the relationship between how often you should sample an input signal and whether you’ll be able to tell what it is when you are finished. It states that in order to represent an input signal, the sampling rate must be at least twice the frequency of the fastest signal. If it’s not then either you won’t be able to recognize the output at all, or you will have the higher-frequency signals "aliasing" and looking like a slower signal. If the sampling is far too slow we to be able to represent the signals accurately, so typically the faster you can sample an input signal the better results you’ll get.

1. The maximum resolution of the ADC is 12-bits. How many quantization steps/values does this give us?

This gives us 4096 quantization steps/values with about 341.333 samples per wave cycle.

1. What are the steps to perform an ADC calibration?

Here are the steps to perform an ADC calibration procedure. First you must ensure that ADEN = 0. Second you set ADCAL = 1. Third and finally you wait until ADCAL = 0. All these bits can be found in the ADC\_CR register.

1. What's the difference between right and left-aligned data in the DAC registers?

Each data register is 15 bits in length. So in the case of 8 and 12 bit right aligned data the data is shifted to be aligned with the most significant bit in the register or bit 15. In the case of left aligned data the 12 bits are aligned with the least significant bit in the register or bit 0. The left-aligned mode is also used for selecting the upper bits of a 16-bit number, allowing the DAC to act on 16-bit data without any conversion or shifting. The left-aligned data benefit is that you can take just the most-significant byte of the register, giving you more precision. The right-aligned data can be used without scaling.

1. What DAC register would you use to write 8-bit right-aligned data? (use the peripheral reference manual)

You would use the DAC\_DHR8R1 register.

1. Name something you found confusing or unclear in the lab manual. (If everything was clear, simply answer that you didn't have any issues.)

The lab and peripheral manual didn’t provide much information about the different between left and right aligned data and their benefits/weaknesses. I would have liked more information about this subject.